WHAT IS CLAIMED IS

1. An AT-command analyzing device, comprising:

a transmitting and receiving portion which receives asynchronous transmission serial data based on a baud-rate clock from a DTE;

a control portion which analyzes the data received by said transmitting and receiving portion;

a baud-rate generating portion which generates the baud-rate clock to be output to said transmitting and receiving portion in accordance with instructions from said control portion;

a measuring portion which measures the span of the start bit of the first character of an AT command transmitted from said DTE based on instructions from said control portion;

a rate analyzing portion which receives a measurement result of said measuring portion, outputs frequency-dividing data for producing a clock for sampling the first character, and also outputs, when the rate of the start bit is more than a preset value, a

flag indicating this matter;

a sampling-clock generating portion which selects, in accordance with whether or not said flag is has been set, the frequency-dividing data from either said rate analyzing portion or said control portion, and produces the sampling clock; and

a shift-register portion which receives data subsequent to the start bit of the first character based on the sampling clock from said sampling-clock generating portion, and holds the received data, which data is then read by said control portion.

2. The AT-command analyzing device as claimed in claim 1, wherein said shift-register portion checks, each time when sampling a bit, whether or not the first character is 'A' or 'a' which corresponds to 41H or 61H in hexadecimal notation, and, when determining that the first character is neither 'A' nor 'a', stops the sampling operation and outputs a flag indicating an error to said control means.

3. The AT-command analyzing device as claimed in claim 1, wherein said shift-register portion stops a sampling operation when, before sampling a bit subsequent to the start bit, the level of the received data of said bit subsequent to the start bit changes from high to low, and outputs a flag indicating an error to said control means.

4. The AT-command analyzing device as claimed in claim 1, wherein said shift-register portion attempts to sample, after sampling the 8 bits subsequent to the start bit, the following stop bit, and, when being not able to detect the stop bit, outputs a flag indicating an error to said control means.

5. The AT-command analyzing device as claimed in claim 1, wherein said sampling-clock generating portion can operate in a one-shot-pulse outputting operation mode other than a sampling-clock generating

mode, whether said sampling-clock generating portion operates in said one-shot-pulse outputting operation mode or said sampling-clock generating mode can be determined in accordance with instructions from said control portion, and said sampling-clock generating portion can output a one-shot pulse as an interrupt signal of said control portion in said one-shot-pulse outputting operation mode.